CLAIMS

1. A memory device comprising:

a first memory cell which includes a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

a second memory cell which includes a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

said first and second memory cells being in contact with each other such that they share a common anode.

2. A memory device as in claim 1 wherein said first cell is stacked on top of said second cell.

3. A memory device as in claim 2 wherein said first and second memory cells are each formed of a layered structure which includes a cathode layer, a fast ion conductor material layer and a anode layer.

4. A memory device as in claim 1 wherein each of said cathodes comprises a layer of tungsten, platinum, titanium, cobalt, aluminum, or nickel.

5. A memory device as in claim 1 wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said conductive layer.

6. A memory device as in claim 5 wherein said middle conductive layer comprises tungsten.

7. A memory device as in claim 2 wherein said stacked first and second memory cells are provided over a conductive plug such that a cathode of said second memory cell is in electrical contact with said conductive plug.

8. A memory device as in claim 7 further comprising a first access transistor for said second memory cell, said conductive plug being in contact with an active region of said access transistor.

9. A memory device as in claim 8 wherein another active region of said first access transistor is electrically coupled to a column line conductor.

10. A memory device as in claim 9 wherein a gate of said first access transistor is connected to a word line conductor.

11. A memory device as in claim 8 further comprises a second access transistor for said first memory cell.

12. A memory device as in claim 2 wherein said upper and lower cells are coupled to different column lines.

13. A memory device as in claim 2 wherein said upper and lower cells are connected to the same column lines.

14. A memory device as in claim 11 further comprising:

a circuit for operating said first and second access transistors separately to individually access each of said upper and lower memory cells.

15. A memory device as in claim 11 further comprising:

a circuit for operating said first and second access transistors together to simultaneously access both cells.

16. A memory device as in claim 1 further comprising:

said fast ion conductor is replaced by a glass capable of writing and reading information in response to applied electrical signals.

17. A method of fabricating a memory device comprising:

forming a first memory cell to include a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

forming a second memory cell to include a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

forming a common anode for both of said first and second memory cells.

18. A method as in claim 17 further comprising:

forming said first memory cell such that it is stacked on said second memory cell.

19. A method as in claim 17 further comprising:

forming each of said first and second memory cells of a layered structure which includes a cathode layer, a fast ion conductor material layer and a anode layer.

20. A method as in claim 17 wherein each of said cathodes comprises a layer of tungsten, platinum, titanium, cobalt, aluminum, or nickel.

21. A method as in claim 17 wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer.

22. A method as in claim 21, wherein said middle conductive layer comprises tungsten.

23. A method as in claim 18 further comprising:

forming said stacked first and second memory cells over a conductive plug such that a cathode of said second memory cell is in electrically coupled with said conductive plug.

24. A method as in claim 23 further comprising a column line conductor electrically coupled to a second active region of said first access transistor.

25. A method as in claim 23 facing a word line conductor which is electrically coupled to a gate of said first access transistor.

26. A method as in claim 23 further comprising forming a second access transistor and electrically coupling said second access transistor to said upper cell.

27. A method as in claim 26 wherein said upper and lower cells are coupled to different column lines by said first and second access transistors.

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28. A method as in claim 17 wherein said upper and lower cells are connected to the same column line by said first and second access transistors.

29. A method as in claim 26 further comprising:

forming a circuit for operating said first and second access transistors separately to individually access each of said upper and lower memory cells.

30. A method as in claim 17 further comprising:

forming a circuit for operating said first and second access transistors together to access both memory cells simultaneously.

31. A computer system comprising:

a processor;

a memory device electrically coupled to said processor, said memory device comprising:

a first memory cell which includes a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

a second memory cell which includes a chalcogenide glass material containing a fast ion conductor and cathode and anode electrodes spaced apart and in contact with said fast ion conductor material;

said first and second memory cells being in contact with each other such that they share a common anode.

32. A memory device as in claim 31 wherein said first cell is stacked on top of said second cell.

33. A memory device as in claim 32 wherein said first and second memory cells are each formed of a layered structure which includes a cathode layer, a fast ion conductor material layer and a anode layer.

34. A memory device as in claim 31 wherein each of said cathodes comprises a layer of tungsten, platinum, titanium, cobalt, aluminum, or nickel.

35. A memory device as in claim 31 wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said conductive layer.

36. A memory device as in claim 35 wherein said middle conductive layer comprises tungsten.

37. A memory device as in claim 32 wherein said stacked first and second memory cells are provided over a conductive plug such that a cathode of said second memory cell is in electrical contact with said conductive plug.

38. A memory device as in claim 37 further comprising a first access transistor for said second memory cell, said conductive plug being in contact with an active region of said access transistor.

39. A memory device as in claim 38 wherein another active region of said first access transistor is electrically coupled to a column line conductor.

40. A memory device as in claim 39 wherein a gate of said first access transistor is connected to a word line conductor.

41. A memory device as in claim 38 further comprises a second access transistor for said first memory cell.

42. A memory device as in claim 32 wherein said upper and lower cells are coupled to different column lines.

43. A memory device as in claim 32 wherein said upper and lower cells are connected to the same column lines.

44. A memory device as in claim 43 further comprising:

a circuit for operating said first and second access transistors separately to individually access each of said upper and lower memory cells.

45. A memory device as in claim 41 further comprising:

a circuit for operating said first and second access transistors together to simultaneously access both cells.

46. A memory device as in claim 31 further comprising:

said fast ion conductor is replaced by a glass capable of writing and reading information in response to applied electrical signals.

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